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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yi Ding  
Assignee: ProMOS Technologies Inc.  
Title: Fabrication Of Gate Dielectric In Nonvolatile Memories In Which A Memory Cell Has Multiple Floating Gates  
Application No.: 10/632,154 Filing Date: July 30, 2003  
U.S. Patent No.: 7,052,947 Issue Date: May 30, 2006  
Examiner: Mathew Smith Group Art Unit: 2812  
Docket No.: M-15230 US

San Jose, California  
November 20, 2007

Attn: Certificate of Correction Branch  
Commissioner For Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Certificate**

NOV 27 2007

PETITION FOR ENTRY OF CERTIFICATE OF CORRECTION of Correction

Sir:

Please enter the enclosed Certificate of Correction (Form PTO 1050) in the above patent.

The errors sought to be corrected were made by the Patent and Trademark Office. Thus, no fee is believed to be required. However, if a fee is required for this submission, please charge the fee to deposit account no. 50-2257.

Please direct all inquiries concerning this request to the undersigned attorney at (408) 392-9250. This form is submitted in duplicate.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 20, 2007.

Michael Shenker 11-20-07  
Attorney for Applicant(s) Date of Signature

Respectfully submitted,

*Michael Shenker*

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U.S. Patent No. 7,052,947

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Page 1 of 1

PATENT NO. : 7,052,947  
APPLICATION NO.: 10/632,154  
ISSUE DATE : May 30, 2006  
INVENTOR(S) : Yi Ding

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On front page, please delete Assignee country "JP" and insert --TW--

Col. 12, line 9 after "(c)" insert --after--

Col. 12, line 11 after "memory cell" insert --, the floating and control gates being provided entirely by the one or more second layers, the floating and control gates comprising no portion of the first layer--

**MAILING ADDRESS OF SENDER (Please do not use customer number below):**

Macpherson Kwok Chen & Heid LLP  
2033 Gateway Place, Suite 400  
San Jose, CA 95110

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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